REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

Examiner rejects Claims 1-11 under 35 U.S.C. 103(a) as being unpatentable over Tsuji in view of Harari. The Examiner states that Tsuji teaches a method of manufacturing a semiconductor device comprising forming an insulating film over a substrate, forming a first mask on said insulating film and specifically refers to col. 5, line 24.

We believe that the Examiner has a misunderstanding because of the utilization of the term "first mask" in the cited reference and the utilization of the term "first mask film" in the present claim. They are not at all equivalent. On lines 24-25, the reference cites "...with the aid of a pattern as a first mask 23, formed so that the exposure light is not irradiated ...". Looking at figures 2A and 2B, it is clear that reference 23 refers to an exposure mask, sometimes called a reticule (as referred to in previous responses) which is utilized to expose the wafer in photolithography processes utilized in manufacturing integrated circuits, as is well known to those skilled in the art. This is why the structure having reference 23 is shown above the surface of the semiconductor and why light is shown impinging on its surface. This feature is clear from col. 5, lines 22-24 which recites utilization of a stepper for the first exposure of the resist layer.

The Examiner states that the reference recites the formation of a resist film on the first mask film and refers to col. 5, line 18. The Examiner states that the resist film serves as a mask during the etching process and refers to col. 5, lines 32-35 which is used to form an opening which is followed by the formation of the trenches on the insulated film.

While applicants agree that the references cites the formation of a resist layer, applicants disagree that the resist layer is formed on a first mask film. The reference states that the resist layer 22 is formed on an interlayer insulating film 21. It is clear from the process shown in figures 2-5 that this interlayer insulating film 21 is not utilized as a mask layer, as it is the layer that is etched and a second resist layer 41 is placed upon the layer 21 prior to the formation of the trenches. It should be noted that the present claims recite the forming of an insulating film, the forming of a first mask film and the forming of a resist film on the first mask film and the utilization of the first mask film in etching the trenches deeper. Applying this to the reference, at best we can see is the formation of both an insulating film and a resist film, but not a first mask film which is utilized in etching the trenches deeper.

Examiner states that Tsuji teaches the formation of a second mask film and refers to col. 5 , line 46 and its use as an etching mask during the formation of connecting holes and refers to col. 5, lines 44-50.

Again, we believe that the recitation of a "second mask" on line 46 and the recitation of a "second mask film" in the present claims has caused the Examiner to be confused. These are not in any way equivalent. On line 46, the second mask is referred to by reference 31. Referring to figures 3A and 3B, it is clear that the structure shown by reference 31 is an exposure mask where the photolithographic process, as described above. In deed, on line 46-48, the reference 31 is described as having "a pattern such that an exposure light beam is irradiated on that region of the resist layer 22 which is on that region of the interlayer insulating film 21 where a contact hole is later formed ..." In sharp contrast, the second insulated film of the present invention is formed on the integrated circuit itself.

The Examiner further states that Tsuji discloses that the second mask is located in the same position where the opening would be later etched. The Examiner states that, "given the fact that the second opening in Applicant's invention is etched through the sidewalls covered with the second mask film, it is the Examiner's position that Tsuji's disclosure about the position of the openings etched after deposition of the second mask reads on Applicant's limitation of "the second mask film covering sidewalls and a bottom of the trenches." (Emphasis added)

Applicants do not agree with the Examiner's interpretation of the claim language. Furthermore , as described above, the "second mask" recited by Tsuji, is not on the semiconductor substrate at all, but is an exposure mask or a reticule used to expose the surface of the semiconductor to irradiating illumination in a photolithographic process. Secondly, the second opening in Applicant's invention is not etched through the sidewalls at all. In fact, the purpose of the sidewalls formed of the second insulating film is to prevent etching through the sidewalls of the trench, see figures 4 and 5. It should be noted that although the trenches shown in Tsuji are shown as having sharply vertical sidewalls, it is a particular problem in the formation of the trenches that the walls are actually tapered. The taper causes the trench to be have an opening that is wider at the top than at the bottom. By covering the sidewalls with a second mask film, the taper is greatly reduced resulting in trenches having much less taper and therefore more substantially vertical sidewalls. This is very important in the semiconductor processes because a certain width of the trench is required for the trench to perform the desired function. If the width of the trench is tapered, the minimum dimension must be met at the bottom of the trench, where the width of the trench is at a minimum, and this requires that the trench have a greater width than desirable at the top. This means that

additional "real estate" on the surface of the chip is required which reduces the number of integrated circuits that can be manufactured on a single wafer, thus dramatically increasing the cost of the process.

In the present invention, the second mask film is removed only at the bottom of the trench, and not along the sidewalls, to eliminate or dramatically reduce this tapering that would be found in the Tsuji process.

The Examiner also recites Harari as disclosing a semiconductor process that includes the formation of a trench, wherein a trench penetrates the substrate and the Examiner states the advantages recited in Harari for this process. The Examiner specifically refers to col. 13, line 30-68 of Harari. This portion of Harari refers to figure 9. However, the key to the invention is really shown in figure 7 and the text starting at col. 8, line 31 through the bottom of the page which describes figure 7. It is clear from this process and this figure that the trench is formed utilizing only a single masking oxide and that after the trench is formed a second film is formed on the side of the trench. Thus, Harari clearly does not show the utilization of the first mask and the second mask film as an etching mask in etching the trenches deeper as recited in the present claims. In view of the fact that the present claims are method claims, all of the method steps must be considered. The combination of both Harari and Tsuji fail to show or suggest this feature. Furthermore, Harari fails to show or suggest the forming of a second mask film; the second film g formed in Harari being an insulating film on the sides of the trench, but it is not utilized as a mask.

Accordingly, neither the references neither singularly or in combination can show or suggest the formation of trenches having the dramatic reduction in taper of the present invention. The advantages of this have been described above.

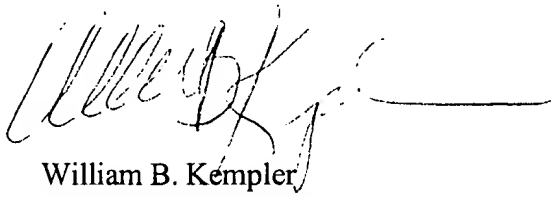
Claims 1 to 3 have been amended in order to clarify the claims by removing the recitation that the trenches are made deeper by the thickness of the insulating film that penetrates into a portion of the substrate, into the last subparagraph of the claim since this is accomplished utilizing the first and second mask film as an etching mask. This feature is clearly supported by referring to figures 2-5 of the present application and the supporting text.

In view of the fact that the difficulties that the Examiner has been having trouble with distinguishing the claims over the cited references is a result of the confusion of the terms "first mask" and "first mask film" and "second mask" and "second mask film", if the Examiner believes that an equivalent term would clarify the claims, the Examiner is invited to call the undersigned for a telephone discussion.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current preliminary amendment. The attached page is captioned "**Marked-up version to show changes.**"

Accordingly, applicants believe the application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,



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MARKED-UP VERSION TO SHOW CHANGES:

1. (~~Three~~ Four Times Amended) A manufacturing method of a semiconductor IC device, comprising the following steps :

forming an insulating film on a semiconductor substrate or SOI substrate;

forming a first mask film on the insulating film;

forming a resist film on the first mask film, the resist film being used as an etching mask to form an opening on the first mask film, followed by the formation of trenches on the insulating film exposed from the opening ~~said trenches being made deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate;~~

forming, after the resist film is removed, a second mask film on the semiconductor substrate or SOI substrate, said second mask film covering side walls and a bottom of the trenches;

removing the second mask film from the bottom of the trenches without removing the second mask film on the side walls of the trenches, forming a side wall made of the second mask film on the side walls of the trenches;

and using the first mask film and the second mask film as the etching mask in etching said trenches deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate ~~so as~~ to form connecting holes.

2. (~~Three~~ Four Times Amended) A manufacturing method of a semiconductor IC device comprising the following steps :

forming an insulating film on a semiconductor substrate or SOI substrate;

forming a first mask film on the insulating film;

forming a resist film on the first mask film, the resist film being used as an etching mask to form an opening on the first mask film, followed by the formation of trenches on the insulating film exposed from the opening ~~said trenches being made deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate;~~

forming , after the resist film is removed, a second mask film on the semiconductor substrate or SOI substrate, said second mask film covering side walls and a bottom of the trenches;

removing the second mask film from the bottom of the trenches without removing the second mask film on the side walls of the trenches, forming a side wall made of the second mask film on the side walls of the trenches;

using the first mask film and the second mask film as the etching mask in etching ~~etching~~ said trenches deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate ~~so as~~ to form an opening on the insulating film, followed by the formation of separating trenches on the semiconductor substrate or SOI substrate exposed from the opening;

burying an insulating film in the separating trenches to form a separating portion.

3. (~~Three~~ Four Times Amended) A manufacturing method of a semiconductor IC device comprising the following steps :

forming an insulating film on a semiconductor substrate or SOI substrate;

forming a first mask film on the insulating film;

forming a resist film on the first mask film, the resist film being used as an etching mask to form an opening on the first mask film, followed by the formation of trenches on the insulating film exposed from the opening ~~said trenches being made deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate;~~

forming, after the resist film is removed, a second mask film on the semiconductor substrate or SOI substrate, said second mask film covering side walls and a bottom of the trenches;

removing the second mask film from the bottom of the trenches without removing the second mask film on the side walls of the trenches, forming a side wall made of the second mask film on the side walls of the trenches;

and using the first mask film and the second mask film as the etching mask in etching said trenches deeper than a thickness of said insulating film so